REMARKS/ARGUMENTS

Examiner Daborah Chacko Davis is thanked for thoroughly reviewing the subject application.

Examiner is also thanked for the indication of allowing claims 1-2 if rewritten of amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office Action.

Examiner is further thanked for allowing claims 4-9, 11-16, 18-23 and 25-30 if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested. All claims are believed to be in condition for allowance.

Claim Rejections - 35 U.S.C. § 112

Reconsideration of the rejection of claims 1-30 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention is respectfully requested based on the following.

The Examiner is thanked for pointing out the various problems of lack of clarity (in claims 1, 5, 12, 19 and 26, further in claims 3, 10, 17 and 24).

The Examiner is further thanked for pointing out problems of lack of antecedent (in claims 3, 4, 7, 10, 11, 14, 17, 18, 21, 24, 25 and 28).

The claims have been carefully reviewed and amended to correct those problems the Examiner pointed out, in addition to others. All claims are now believed to be in allowable condition.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-30 under 35 U.S.C. 112, second paragraph, be withdrawn.

Claim Rejections - 35 U.S.C. § 102

Reconsideration of the rejection of claims 3, 10, 17 and 24 under 35 U.S.C. 102(b) as being anticipated by IBM Technical Disclosure Bulletin (NA8909149) is respectfully requested based on the following.

IBM Technical Disclosure Bulletin (NA8909149) provides for, quoting in abbreviated form and copying from the quoted IBM Bulletin:

- providing a substrate over which a topography has been created, the topography comprising semiconductor devices or semiconductor elements, specifically comprising patterned metal interconnects
- depositing a layer of passivation over the topography
- coating a first layer of photoresist over the layer of passivation, including the patterned metal interconnects

- subjecting the deposited first layer of photoresist to deep UV exposure, ensuring thermal stability of and hardening the first layer of photoresist

- coating a second layer of photoresist over the first layer of photoresist

- creating vias through the first and second layers of photoresist

- applying thermal reflow to the sidewalls of vias created through the second layer of photoresist, the thermally stabilized and hardened first layer of photoresist prevents via shift, and

- transferring the CD of the vias created through the first and second layers of photoresist to an underlying layer of passivation.

The above highlighted procedure, provided by IBM and described in the above referenced publication, assures good photoresist sidewall slopes with minimal or no image shift or size reduction of the vias created through the first and second layers of photoresist.

The above highlighted IMB procedure will be compared with the rejected claims 3, 10, 17 and 24. In the interest of brevity

claim 3 will be (arbitrarily) selected for purposes of providing this comparison and as being representative of the remaining claims 10, 17 and 24 in the group of rejected claims.

Claim 3, which provides a method of the claimed invention for changing of a Critical Dimension in a layer of photoresist that is used for creation of device features that collectively comprise a semiconductor device, will be quoted below. Underlined in this quote will be those aspects of the claimed invention that are not provided by the IBM invention, making the claimed invention patentable over the referenced IBM invention, as follows:

- providing a substrate, the substrate having been provided with semiconductor devices, at least one layer of semiconductor material having been deposited over the substrate, the at least one layer of semiconductor material being patterned for creation of device features of semiconductor devices created on the substrate
- creating a patterned layer of photoresist (NOTE: **a or one**, not two layers of photoresist as provided by the IBM procedure) having a surface over the at least one layer of semiconductor material, creating at least one opening through the layer (NOTE: **the** layer, not two layers as provided by the

IBM procedure) of photoresist having sidewalls having an angle of intersect with the at least one layer of semiconductor material, the at least one opening comprising a via hole and an interconnect line trench, and

- changing the angle of intersect of the sidewalls of the at least one opening created in the patterned layer of photoresist (NOTE: **the** patterned layer of photoresist, not two layers of photoresist as provided by the IBM procedure) by raising a temperature of the layer of the patterned layer of photoresist while placing the surface of the patterned layer of photoresist **under an angle with a horizontal plane,** the horizontal plane coinciding with the plane of the earth's surface.

An inverse comparison can also be made, using the previously provided summary of the IBM procedure for this purpose and underlining in this summary those aspects of the IBM procedure that are not provided by the claimed invention, as follow:

- providing a substrate over which a topography has been created, the topography comprising semiconductor devices or semiconductor elements, specifically comprising patterned metal interconnects
- depositing a layer of passivation over the topography

- coating a **first** layer of photoresist over the layer of passivation, including the patterned metal interconnects

- subjecting the deposited first layer of photoresist to deep UV exposure, ensuring thermal stability of and hardening the first layer of photoresist

- coating a **second** layer of photoresist over the first layer of photoresist

- creating vias through the first and second layers of photoresist

- applying thermal reflow to the sidewalls of vias created through the second layer of photoresist, **the thermally stabilized and hardened first layer of photoresist prevents via shift**

- transferring the CD of the vias created through **the first and second layers** of photoresist to an underlying layer of passivation.

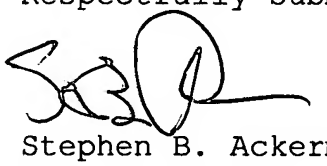
In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of claims 3, 10, 17 and 24 under 35 U.S.C. 102(b) as being anticipated by IBM Technical Disclosure Bulletin (NA8909149), be withdrawn.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

It is requested that, should Examiner not find the claims to be allowable, to call the undersigned Attorney at the Examiner's convenience at 845-452-5863 in order to overcome any problems preventing allowance of the claims.

Respectfully submitted,



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